

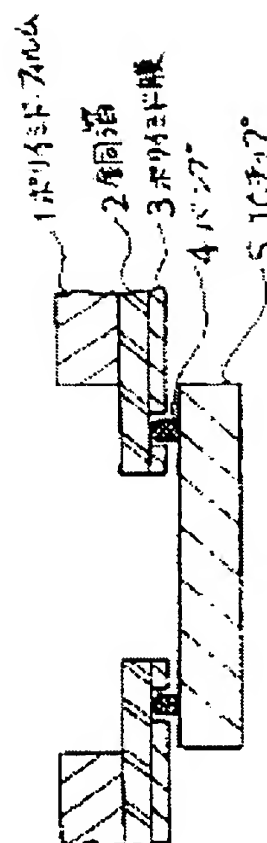
**ASSEMBLY TAPE OF INTEGRATED CIRCUIT DEVICE**

**Patent number:** JP1205544  
**Publication date:** 1989-08-17  
**Inventor:** IWAMATSU SEIICHI  
**Applicant:** SEIKO EPSON CORP  
**Classification:**  
- **international:** H01L21/60  
- **european:**  
**Application number:** JP19880030278 19880212  
**Priority number(s):**

**Abstract of JP1205544**

**PURPOSE:** To eliminate the contact of a lead wire and a defect due to a short circuit and to change a position of a bonding part by forming an insulating film on the surface of a conductor foil sheet excluding a pad part and a part to be bonded to an external lead.

**CONSTITUTION:** A copper foil sheet 2 is formed on the surface of a polyimide film 1; a punched hole is made in the film 1; a lead wire is projected inside the punched hole by the copper foil sheet 2. A polyimide film 3 is coated and formed on the main surface of the copper foil sheet 2 excluding a part where a bump 4 of an IC chip 5 is to be bonded. By this setup, the contact of a lead wire and a defect due to a short circuit are eliminated; a position of a bonding part can be changed.



Data supplied from the **esp@cenet** database - Patent Abstracts of Japan

**BEST AVAILABLE COPY**